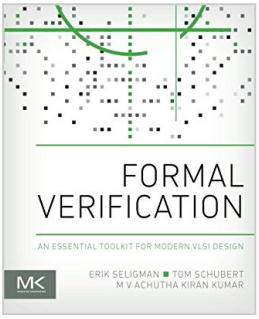

Formal Verification: An Essential Toolkit for Modern VLSI Design

By Erik Seligman, Tom Schubert, M V Achutha Kiran Kumar

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Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity.

- Learn formal verification algorithms to gain full coverage without exhaustive simulation
- Understand formal verification tools and how they differ from simulation tools
- Create instant test benches to gain insight into how models work and find initial bugs
- Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems

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Editorial Review

Review
"...the authors thoroughly expressed their practical knowledge of this complex, and misunderstood topic, in an easy to read presentation...I strongly recommend this book to design and verification engineers who are contemplating, or are currently using formal verification..." --**VerificationAcademy.com**

From the Back Cover
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About the Author
Erik has worked at Intel Corporation in Hillsboro, Oregon for over two decades, in a variety of positions involving software, design, simulation, and formal verification. Currently he works in the Design Technology and Solutions division, where he supports formal verification usage for Intel teams worldwide. In his spare time he hosts the “Math Mutation” podcast, and serves as an elected director on the Hillsboro school board.

Tom recently joined the Electrical and Computer Engineering faculty at Portland State University and directs a graduate track in Design Verification and Validation. Previously, he was at Intel Corporation for 17 years in Hillsboro, Oregon, where he managed Intel's largest pre-silicon validation formal verification team develop and apply FPV techniques on multiple generations of microprocessor designs. Tom received a PhD in Computer Science from the University of California, Davis.

Kiran has been working at intel India for past 11 years and has worked in various areas of the chip design cycle which includes RTL design, structural design, circuit design, simulation and various levels of verification including formal verification. Currently he leads the formal verification efforts for the graphics design in Visual Platform Group and supports formal verification at intel india site.

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