Powerpc System Architecture (PC System Architecture Series)

By Tom Shanley

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PowerPC step-by-step from a system point of view.

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Editorial Review

From the Back Cover

supervisor privilege level facilities

logical memory addresses I/O and memory-mapped I/O

address translation for segments, pages, and blocks virtual paging interrupts

The second half of the book examines the PowerPC 601 processor as an example, exploring how the processor fits, adheres to, and deviates from the PowerPC processor specification. In addition, a detailed discussion of the bus structure and transaction protocol used by the 60x processors is provided.

If you design or test hardware or software that involves PowerPC systems, PowerPC System Architecture is an essential, time-saving tool.

The PC System Architecture Series is a crisply written and comprehensive set of guides to the most important PC hardware standards. Each title is designed to illustrate the relationship between the software and hardware and explains thoroughly the architecture, features, and operations of systems built using one particular type of chip or hardware specification.

The PC System Architecture Series features step-by-step descriptions and instructions and accessible illustrations that enable a wide range of readers to easily understand difficult hardware topics. The authors, expert hardware training consultants for clients including IBM, Intel, Compaq, and Dell, have mastered the art of pinpointing and succinctly explaining just the critical information that PC programmers, software and hardware designers, and engineers need to know and leaving out the rest. The result is an exciting series of books that will enable readers of a wide range of backgrounds to make immediate gains in programming productivity.

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